REMARKS

File History

In the latest substantive Office action of 9/19/2005, the following rejections, objections and other actions appear to have been made:

- Claims 1, 10-15 were rejected under 35 USC §103(a) as being obvious over **Nishioka** et al (US 6,657,249 based on a US application filed 7/8/2002) as combined with **Rabkin** et al (US 6,812,515 based on a US application filed 11/26/2001).

- Claims 2, 10-13 were rejected under 35 USC §103(a) as being obvious over **Nishioka** as combined with **Rabkin** and further in view of **Kobayashi** (US 6,346,448).

- Claims 3-4 were rejected under 35 USC §103(a) as being obvious over **Nishioka** as combined with **Rabkin** and further in view of **Lee** (US2005/0074982 which is a divisional of an earlier application filed 2/2/2001).

- Claims 5-6 were rejected under 35 USC §103(a) as being obvious over **Nishioka** as combined with **Rabkin** and **Lee** and further in view of **Yamazaki** (US2005/0040401 which is a divisional of an earlier application filed 2/22/2000).

- Claims 7-9 were rejected under 35 USC §103(a) as being obvious over **Nishioka** as combined with **Rabkin** and **Lee** and **Yamazaki** and further in view of **Yu** (US 6,566,205 based on a US application filed 1/11/2002).

- Claims 10-11 were additionally rejected under 35 USC §112 for indefiniteness.

- Claims 2-11 were additionally objected for containing parenthetical paragraph markers.

- The restriction was made final.

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Summary of Current Response

Claim 22 is newly introduced.

Claims 16-21 are canceled without prejudice.

Arguments are presented concerning the applied art and its proposed combination.

Applicants' Overview of Outstanding Office Action

Applicant sees the outstanding Office action of 9/19/2005 ("OA") as having the following major features:

(1) A critical fact finding error underlies all rejections. The PTO finds that region 106 of **Nishoka** '249 is produced by oxidizing at least a sublayer portion of a first intrinsic silicon layer so as to thereby create a corresponding and thermally-grown, first intrinsic silicon oxide sublayer.

(2) A critical error regarding motivation for combining underlies all rejections. The PTO finds that one skilled in the art would have been motivated to improve conduction between control and floating gates of a memory device. At OA page 4, last few lines the PTO asserts:

> Rabkin et al disclose ... 206 and ... 208 are doped-polysilicon. ... Therefore it would have been obvious ... to dope the semiconductor layers of Nishioka ... *for the purpose of better conducting between the **floating** gate* and control gate .... [*Emphasis added.*]

(3) No legal basis exists for the indefiniteness rejections or objections to claim format.

In view of the above, it is respectfully submitted that a prima facie case of unpatentability has not been made out.

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Definition of "intrinsic"

The term "intrinsic" appears in the rejected claims. At paragraph [0016] of the specification, it is stated:

> This nitridated surface will serve as an oxidation stop. A thin film of **intrinsic (essentially undoped)** silicon is then deposited on the Si_xN_y surface. Heat and an oxidizing atmosphere are then provided for converting the deposited, intrinsic silicon into a thermally-grown oxide layer (Si_mO_n , where typically m=1 and n=2). [*Emphasis added*]

At paragraph [0017] of the specification, it is stated:

> Charge leakage between the floating gate (FG) and the control gate (CG) of this embodiment is reduced because the thermally-grown and **dopant-free** oxide portion of the NONO structure exhibits good insulating properties, particularly because it is grown from **intrinsic** silicon. [*Emphasis added*]

Online dictionaries give the following ordinary meanings for "intrinsic":

> **intrinsic**: b : being or relating to a semiconductor in which the **concentration of charge carriers is characteristic of the material itself instead of the content of any impurities** it contains [from http://www.m-w.com/cgi-bin/dictionary?book=Dictionary&va=intrinsic on or around Oct. 24, 2005, emphasis added]
>
> Of or relating to the essential nature of a thing; inherent. [from another internet source on same date]

Background on Technology and Comment re Erroneous Motivation to Combine

At paragraph [0012] of the specification, it is stated:

> Practitioners in the art have developed a so-called ONO solution. According to basic ONO practice, after the material for the floating gate (FG) is deposited (typically it is doped polysilicon), three insulative layers are vapor deposited in sequence. The three insulative layers are respectively composed of silicon-Oxide, silicon-Nitride and silicon-Oxide; **hence the ONO acronym**. The material for the control gate (CG) is then deposited (typically it is doped polysilicon) on top of the ONO structure. [Emphasis added]

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

Those skilled in the art readily understand that the ONO stack helps to keep the control gate of the memory device desirably insulated from the "floating" gate. The latter is termed "floating" because it is designed to be insulated from surrounding conductive structures.

Applicant is therefore taken aback by a motivation-to-combine argument proffered by the PTO at OA page 4: "Therefore it would have been obvious ... to dope the semiconductor layers of Nishioka ... for the purpose of better conducting between the floating gate and control gate ...." (emphasis added). This is contrary to basic understandings of those skilled in the art. Accordingly, the articulated motivation to combine Nishioka with Rabkin is fatally flawed and should be withdrawn.

Since all outstanding, art-based grounds of rejection are founded on the erroneous combination of Nishioka with Rabkin, they should all be withdrawn.

Other Erroneous Fact Finding

Another foundational error that underlies all of the art-based rejections deals with item 106 of Nishioka. Nishioka col. 1, lines 28-45 explain:

> FIG. 34 shows the memory transistor 150 of the memory cell part R1 in two sections along bit and word lines respectively. **An n-conductivity type bottom well 103** is provided at a **part of the bottom of a silicon substrate 101** ... The memory cell **transistor** 150 has source and drain regions 108a and 180b formed in the **p-conductivity type well 105** and a gate insulator film 106 ... [*emphasis added*]

By contrast, at OA page 4, lines 1-etc., the PTO implies that the silicon substrate 101 of Nishioka constitutes intrinsic silicon (essentially undoped silicon). Those skilled in the art would understand that this is not so merely from viewing Nishioka Fig. 34. Moreover, Nishioka expressly states that portion 103 of the substrate 101 is n-doped.

At OA page 4, lines 1-etc., the PTO further implies that layer 106 of Nishioka Fig. 34 constitutes the intrinsic silicon dioxide layer thermally grown on P-well 105. Since well 105 is

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

a p-doped region, this simply cannot be true. Moreover, nowhere does Nishioka expressly teach that the gate oxide layer 106 is thermally grown from intrinsic silicon. Instead at col. 2, lines 1- ... Nishioka teaches:

> **First**, the element isolation zone 102 is formed on the **main surface of the p-conductivity type silicon substrate 101** having <100>crystal orientation (see FIG. 35). ...
>
> Then, the **p-conductivity type well regions 105** are formed in the region of the peripheral circuit part R2 ... [when] (a) Boron is ion-implanted with acceleration energy of 700 keV and ....
>
> ***Thereafter*** a silicon oxide **film 106** of about 10 nm in thickness *is formed* on the main surface of the silicon substrate 101 **by thermal oxidation**. Then, a phosphorus-doped polycrystalline silicon film 107 of about 200 nm in thickness is formed. Thereafter a resist pattern is formed on the overall main surface of the silicon substrate 101 by photolithography. This resist pattern is employed as a mask for patterning the phosphorus-doped polycrystalline silicon film 107 thereby forming the floating gate 107 on the region to be formed with the memory transistor 150. [emphasis added]

Thus it is indisputable that element 106 of Nishioka is formed by thermal oxidation of p-doped "main surface" of substrate 101 after p-wells 105 have been formed.

In view of the above, it is clear that errors have been made with respect to the teachings of Nishioka and the motivation to combine with Rabkin. All art-based rejections rest on the foundation of Nishioka combined with Rabkin. Therefore all must fall.

Traverse of Indefiniteness Rejections

These rejections apply only to claims 10-11.

No disrespect is intended, but Applicant should not be put in a position of having to instruct Examiners in the English language. In Claim 10, the verb is "continuing" and the modifying clause for this action is "at least until a corresponding first oxidation front crosses

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

into the first oxidation stop layer". Those skilled in the art will understand that oxidation did not have to continue to that point and instead could have been stopped earlier. Those skilled in the art will understand that by continuing oxidation all the way through, more silicon is joined with oxygen to thereby form more stoichiometric silicon dioxide and to thereby perfect formation of good insulator. There is nothing indefinite in this recital.

With regard to Claim 11, persons skilled in the art normally expect oxidation to stop when the front hits the stop layer. However, the inventors believe that further silicon can be converted into silicon oxide by continuing oxidation temperature even after the front has hit the stop layer. There is nothing indefinite in the recital of this apect.

Traverse of Format Objections

While Examiners have broad discretion and thus great power, they do not have power to arbitrarily make up their own rules. There is no rule against use of parenthetical notations to indicate how limitations are organized. Paragraph (c) of Claim 1 recites "oxidizing at least a sublayer portion of the first intrinsic silicon layer". Paragraph (c.1) of Claim 2 further narrows this aspect by requiring that "said thermally-grown, first intrinsic silicon oxide sublayer includes stoichiometric silicon dioxide (SiO2)."

With regard to the preambles of the claims, the basis of objection is not stated.

Given that all outstanding rejections are founded on the above-identified, incorrect reading of Nishioka and/or on unsupported non-art bases, they should all be withdrawn.

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262

CONCLUSION

In light of the foregoing, Applicant respectfully requests that the rejections be withdrawn. Should any other action be contemplated by the Examiner, it is respectfully requested that he contacts the undersigned at (408) 392-9250 to discuss the application.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time and/or fee for additional claims, which may be required.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on _October___27____, 2005.

	10/26/05
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,

Gideon Gimlan
Attorney for Applicants
Reg. No. 31,955

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive, Suite # 226
San Jose, CA 95110
Tel: (408) 392-9250

MacPherson Kwok Chen & Heid LLP
1762 Technology Drive,
Suite 226
San Jose, CA 95110
Telephone: (408) 392-9250
Facsimile: (408) 392-9262